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SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT I, Kiyoshi Irino, a citizen of Japan residing at Kawasaki-shi, Kanagawa, Japan have invented certain new and useful improvements in

SEMICONDUCTOR MEMORY DEVICE CONTAINING NITROGEN IN A GATE OXIDE FILM

of which the following is a specification : -

1 TITLE OF THE INVENTION

SEMICONDUCTOR MEMORY DEVICE CONTAINING
NITROGEN IN A GATE OXIDE FILM

5 BACKGROUND OF THE INVENTION

The present invention generally relates to fabrication of semiconductor devices and more particularly to fabrication and construction of a high speed field-effect transistor.

10 High-speed logic integrated circuits
generally use high-speed CMOS circuits. CMOS circuits
consume little electric power and are particularly
suited for this purpose. In order to increase the
operational speed of high-speed CMOS circuits further,
15 a very fast field-effect transistor is needed.

Conventionally, the operational speed of a field-effect transistor has been increased mainly by reducing the gate length, which in turn is achieved by a device miniaturization. For example, MOS transistors having a gate length as small as $0.35\text{ }\mu\text{m}$, are used these days for such high performance applications.

On the other hand, further reduction of gate length is generally difficult in MOS transistors, as carriers tend to experience excessive acceleration in a channel region immediately under a gate electrode of the MOS transistor when the gate length of the MOS transistor is thus reduced. The carriers thus accelerated tend to penetrate into a gate oxide film and form fixed electric charges therein, while such fixed electric charges tend to modify the threshold characteristics of the MOS transistor.

In more detail, the carriers thus penetrated into the gate oxide film enter the SiO_2 structure that form the gate oxide film, wherein the carriers thus penetrated into the SiO_2 structure are held stably when the carriers are captured by the dangling bonds

1 of the SiO_2 structure.

Thus, it has been practiced conventionally in the art of MOS transistors to terminate any dangling bonds existing in the gate oxide film by 5 introducing N atoms thereinto, so that the number of the sites which may capture the carriers is reduced as much as possible.

FIGS.1A - 1D show a conventional fabrication process of a MOS transistor.

10 Referring to FIG.1A, a field oxide film 2 is formed on a Si substrate 1 doped to the p-type or n-type, such that the field oxide film 2 defines a device region 1A on the surface of the substrate 1. The field oxide film 2 is typically formed by a wet etching process with a thickness of 300 - 400 nm. 15 Further, a thermal oxide film 3 is formed on the Si substrate 1 so as to cover the device region 1A with a thickness of typically about 6 nm. The thermal oxide film 3 acts as a gate oxide film of the MOS transistor to be formed.

20 The structure of FIG.1A is then annealed in an N_2O atmosphere at a temperature of typically 800°C , such that N atoms in the atmosphere are incorporated into the gate oxide film 3.

25 Next, in the step of FIG.1B, a polysilicon film 4 is deposited on the structure of FIG.1A by a CVD process conducted at a temperature of $800 - 900^\circ\text{C}$, typically with a thickness of about 150 nm. Further, 30 the polysilicon film 4 is patterned in the step of FIG.1C by an anisotropic etching process such as an RIE (reactive ion etching) process, and a gate electrode 4A is formed as a result.

35 After the gate electrode 4A is thus formed, an ion implantation process of a p-type dopant such as B or an n-type dopant such as As or P is introduced into the substrate 1 while using the gate electrode 4A as a mask. Thereby, diffusion regions 1B and 1C are

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1 formed in the substrate 1 respectively in
correspondence to a source region and a drain region
of the MOS transistor to be formed. Further, a CVD-
SiO₂ film 5 is deposited on the structure thus
5 obtained by a CVD process conducted at the temperature
of 800 - 900°C, typically with a thickness of about
100 nm.

Next, in the step of FIG.1D, the CVD-SiO₂
film 5 is subjected to an anisotropic etching process
10 that acts substantially vertically to the principal
surface of the substrate 1, and side wall oxides 5A
and 5B are formed at respective lateral sides of the
gate electrode 4A. Further, by carrying out the ion
implantation process of the p-type dopant or the n-
15 type dopant once more into the substrate 1 in the
state that the gate electrode 4A carries the side wall
oxides 5A and 5B, further diffusion regions 1B' and
1C' having a higher dopant level are formed inside the
diffusion regions 1B and 1C. In other words, the MOS
20 transistor thus formed has a so-called LDD (lightly
doped drain) structure.

It should be noted that, in the MOS
transistor of the foregoing structure, the gate oxide
film 3 acts as an etching stopper when patterning the
25 gate electrode 4A. Thereby, the part of the gate
oxide film 3 not protected by the gate electrode 4A
may experience an increased degree of damage during
the etching process. For example, the Si-O bonds in
the SiO₂ structure of the gate oxide film 3 may be
30 broken.

When such breaking of the Si-O bond occurs,
dangling bonds are formed inevitably in the structure
of the gate oxide film 3, while it is known that the
dangling bonds tend to capture H or OH ions. In the
35 case of the high speed MOS transistor of FIG.1D that
has a short channel length, there is a substantial
risk that the dangling bonds in the gate oxide film 3

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1 capture the hot carriers that are accelerated at the
edge of drain region 1C and penetrated into the gate
oxide film 3 as indicated in FIG.2, wherein FIG.2
shows the drain region 1C in an enlarged scale.

5 In order to overcome the problem, it has
been proposed to introduce N atoms into the gate oxide
film 3 in the process of FIG.1A, such that the N atoms
thus introduced terminate the dangling bonds in the
10 gate oxide film 3. As a result of such a process, the
trapping of the hot electrons by the dangling bonds is
reduced substantially.

15 On the other hand, the conventional process
of FIGS.1A - 1D raises a problem in that, because the
N atoms are introduced at a relatively early phase of
the process, the N atoms thus incorporated easily
20 escape in the following processes, particularly those
including thermal annealing processes. In other
words, it has been necessary in the conventional
process of FIGS.1A - 1D to incorporate a very large
amount of N atoms into the gate oxide film 3 in order
that such a doping by the N atoms is effective for
suppressing the trapping of the hot carriers by the
dangling bonds.

25 When the N atoms are introduced in the step
of FIG.1A, it should be noted that the N atoms are
introduced not only into the part of the gate oxide
film 3 corresponding to the edge part of the drain
region as shown in FIG.2 but also into the part
immediately underneath the gate electrode 4A.
30 Thereby, the MOS transistor thus obtained tends to
show a threshold characteristic substantially
different from the desired or designed threshold
characteristic.

FIGS.3A and 3B show a flat-band voltage V_{FB}
35 and a threshold voltage V_{TH} of the MOS transistor for
the case in which the gate oxide film, formed as a
result of a thermal oxidation process in a dry O_2

1 environment, is exposed to various N-containing
atmospheres at a temperature of about 800°C.

Referring to FIGS.3A and 3B, it will be noted that both the V_{FB} and the V_{TH} are modified significantly as a result of the thermal annealing process conducted in the NO or N_2O atmospheres for various durations. As already noted, the concentration of the N atoms in the gate oxide film 3 is changed substantially by the heating processes included in the steps of FIGS.1A - 1D. Thus, it has been difficult in the conventional MOS transistor, fabricated according to the process of FIGS.1A - 1D, to control the characteristics thereof exactly, and there has been a problem in that the transistor shows a large scattering of the characteristics. This problem becomes particularly acute in the MOS transistors in which a very large amount of N atoms are introduced into the gate oxide film for effective termination of the dangling bonds therein.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide a novel and useful semiconductor device and a fabrication process thereof wherein the foregoing problems are eliminated.

Another and more specific object of the present invention is to provide a semiconductor device and a fabrication process thereof, wherein the problem of trapping of the hot carriers in the gate oxide film is successfully eliminated while simultaneously realizing a stable and reproducible device characteristic.

Another object of the present invention is to provide a semiconductor device, comprising:

35 a substrate;
a gate oxide film formed on said substrate;
a gate electrode provided on said gate oxide

1 film;

first and second diffusion regions formed in said substrate at both lateral sides of said gate electrode;

5 said gate electrode including a first region located immediately underneath said gate electrode and a second region adjacent to said first region, said first and second regions containing N atoms with respective concentrations such that said second region 10 contains N with a higher concentration as compared with said first region.

According to the present invention, the variation of the threshold or other characteristic of the semiconductor device is successfully suppressed while simultaneously suppressing the problem of the trapping of the hot carriers in the gate oxide film in the vicinity of the drain edge.

Another object of the present invention is
to provide a method of fabricating a semiconductor
device, comprising the steps of:

forming a gate oxide film on a substrate;
forming a gate electrode pattern on said
gate oxide film; and
introducing N atoms into said gate oxide
film while using said gate electrode pattern as a
mask.

According to the present invention, the N atoms are introduced into the gate oxide film selectively in correspondence to the edge part of the drain region where the acceleration of the carriers, and hence the formation of the hot carriers, is maximum, while the gate oxide film immediately underneath the gate electrode pattern is maintained substantially free from the N atoms. Thereby, the problem of trapping of the hot carriers in the gate oxide film is successfully avoided in the part where the creation of the hot carriers is maximum. As the

1 gate oxide film is substantially free from the N atoms
in the part immediately underneath the gate electrode
pattern, the designed operational characteristic is
obtained for the semiconductor device with reliability
5 and reproducibility.

Other objects and further features of the present invention will become apparent from the following detailed description when read in conjunction with the attached drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIGS.1A - 1D are diagrams showing a conventional fabrication process of a semiconductor device;

15 FIG.2 is a diagram explaining the problem
pertinent to the conventional semiconductor device;

FIGS. 3A and 3B are further diagrams explaining the problem of the conventional semiconductor device;

20 FIG.4 is a diagram showing the principle of
the present invention;

FIGS. 5A - 5G are diagrams showing a fabrication process of a semiconductor device according to a first embodiment of the present invention:

FIG.6 is a diagram showing a distribution profile of N atoms in a gate oxide film of the semiconductor device of the first embodiment;

FIGS. 7A - 7G are diagrams showing a
30 fabrication process of a semiconductor device
according to a second embodiment of the present
invention; and

FIG.8 is a diagram showing the effect of the present invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS
[PRINCIPLE]

1 FIG. 4 shows the principle of the present
invention, wherein those parts corresponding to the
parts described previously are designated by the same
reference numerals and the description thereof will be
5 omitted.

Referring to FIG.4, the present invention introduces N atoms into a part of the gate oxide film 3 indicated by a hatched region selectively with respect to the adjacent region located immediately underneath the gate electrode pattern 4A. Thereby, it should be noted that the N atoms are contained mostly in the hatched region and the concentration of the N atoms in the adjacent region is held minimum. Thus, the problem of modification of the threshold characteristics of the semiconductor device by the N atoms thus doped into the gate oxide film 3 is effectively and successfully minimized.

20 In the construction of FIG.4, it should be noted that the N atoms are introduced selectively and with a high concentration level into the region that tends to experience most severe damages during the patterning process of the gate electrode pattern 4A. Further, the region of the gate oxide film 3 where the N atoms are introduced selectively corresponds to the 25 part of the channel region where the creation of the hot carriers is maximum. Thus, any dangling bonds that are created as a result of the damage are immediately terminated by the N atoms and the problem of trapping of the hot carriers by the dangling bonds 30 is successfully eliminated.

As the foregoing doping of the N atoms into the gate oxide film 3 is achieved after the deposition and patterning of the gate electrode pattern 4A, the problem of escaping of the N atoms by the heat caused during the deposition of the gate electrode pattern 4A is successfully avoided.

Further, when the doping of the N atoms is

1 conducted by exposing the gate oxide film 3 to the NO
atmosphere, the subsequent process of depositing the
side wall oxides 5A and 5B may be conducted
immediately thereafter, in the same deposition
5 apparatus, continuously and without exposing the
substrate to the environment. It should be noted that
the annealing process for introducing the N atoms is
conducted at the temperature of about 800°C, while
this temperature is the temperature used for
10 depositing the side wall oxides 5A and 5B by way of a
CVD process.

[FIRST EMBODIMENT]

15 FIGS.5A - 5G show the fabrication process of
a MOS transistor according to a first embodiment of
the present invention.

Referring to FIG.5A, a Si substrate 11
corresponding to the Si substrate 1 of FIG.1A is
20 formed with a well 11a of the p-type or n-type, and a
field oxide film 12 is formed on the substrate 11 by a
wet oxidation process with a thickness of typically
300 - 400 nm, such that the field oxide film 12
defines a device region 11A on the surface of the
substrate 11. Further, a thermal oxide film 13 is
25 formed on the substrate 11 so as to cover the device
region 11A with a thickness of typically 6 nm.

Further, in the step of FIG.5B, a
polysilicon film 14 corresponding to the polysilicon
film 4 of FIG.1B is deposited on the structure of
30 FIG.5A typically with a thickness of about 15 nm by a
CVD process conducted at a temperature of 800 - 900°C.
The polysilicon film 14 thus formed is then subjected
to an anisotropic etching process such as an RIE
process in the step of FIG.5C and a gate electrode 14A
35 is formed.

In the step of FIG.5C, a p-type dopant such
as B or an n-type dopant such as As or P is further

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1 introduced into the substrate 11 by an ion
implantation process while using the gate electrode
14A as a mask, and diffusion regions 11B and 11C are
formed in the substrate 11.

5 Further, the substrate 11 thus processed is
introduced into a CVD apparatus and exposed to an
atmosphere containing NO for a duration of typically 5
- 20 minutes. Because of the toxic nature of NO, it
is preferable to use a diluted gas of NO for the
10 foregoing exposure process in which NO is diluted in
an Ar carrier gas with a volumetric concentration of
about 30%. Further, it is desirable, for the sake of
safety, to carry out the exposure under a reduced
pressure environment of about 40 Pa, for example.

15 As a result of the thermal annealing applied
during the exposure process, the impurity elements
introduced previously by the ion implantation process
cause a diffusion into the substrate 11 and the
diffusion regions 11B and 11C noted previously are
20 formed as a result of such a diffusion of the impurity
element. Thus, the annealing process associated with
an ion implantation process is achieved simultaneously
to the thermal annealing process for introducing the N
atoms in the present embodiment.

25 Next, in the step of FIG.5D, a CVD-SiO₂ film
15 is deposited on the structure of FIG.5C by a CVD
process conducted in the same CVD apparatus at a
temperature of typically about 800 °C, with a
thickness of about 100 nm. It should be noted that
30 the CVD process of FIG.5D is conducted continuously to
the exposure process of FIG.5C.

Next, in the step of FIG.5E, the CVD-SiO₂
film 15 is subjected to an anisotropic etching process
such as an RIE process acting substantially
35 perpendicularly to the principal surface of the
substrate 11, and side wall oxides 15A and 15B are
formed at both lateral sides of the gate electrode

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1 14A, similarly to the side wall oxides 5A and 5B of
2 FIG.1D. Further, by conducting an ion implantation
3 process of the foregoing p-type or n-type dopant into
4 the substrate 11 in the state that the gate electrode
5 14A carry the side wall oxides 15A and 15B, an LDD
6 structure including diffusion regions 11B' and 11C'
7 having a higher impurity concentration level inside
8 the diffusion regions 11B and 11C, are obtained.

9 Next, in the step of FIG.5F, an interlayer
10 insulation film 16 of SiO_2 is deposited on the *As shown in*
11 *Fig.5G* structure of FIG.5E with an appropriate thickness, and
12 ohmic electrodes 17A and 17B are provided on the
13 interlayer insulation film 16 in ohmic contact with
14 the diffusion regions 11C and 11B respectively via
15 contact holes formed in the interlayer insulation film
16.

16 In the present embodiment, the process of
17 FIG.5C for introducing the N atoms into the gate oxide
18 film 13 is carried out while using the gate electrode
19 14A as a mask. Thus, the incorporation of the N atoms
20 does not occur in the part of the gate oxide film 13
21 located immediately underneath the gate electrode 14A
22 and covering the channel region. Thus, no substantial
23 change occurs in the threshold characteristic or flat-
24 band characteristic of the MOS transistor even when
25 the N atoms are introduced into the gate oxide film
13.

26 As the N atoms are introduced with a high
27 concentration level selectively into the part of the
28 gate oxide film 13 corresponding to the drain edge
29 where the creation of the hot-carriers is most
30 prominent, the dangling bonds in the SiO_2 structure
31 forming the gate oxide film 13 are effectively
32 terminated, and the sites for trapping hot-carriers
33 are annihilated. Thus, the problem of trapping of the
34 electrons or holes by the gate oxide film 13 is
35 successfully avoided.

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1 In the step of FIG.5C, it should be noted
that the exposure process may be conducted in an
atmosphere containing N₂O in place of NO. In this
case, it is preferable to use the annealing
5 temperature of about 900°C, rather than 800°C.
Generally, the amount of the N atoms incorporated into
the gate oxide film 13 is reduced when the exposure is
carried out in the N₂O atmosphere rather than in the
NO atmosphere. When N₂O is used in the step of
10 FIG.5C, it is necessary to lower the temperature of
the CVD apparatus to about 800 °C when carrying out
the CVD process of FIG.5D. Such thermal annealing
processes at different temperatures can be conducted
efficiently by using a cluster-type processing
15 apparatus.

FIG.6 shows the distribution profile of N
atoms in the depth direction of the gate oxide film 13
as measured by a SIMS (secondary ion mass
spectroscopy) analysis.

20 Referring to FIG.6, it should be noted that
the concentration level of the N atoms is much higher
when the thermal annealing process is conducted in the
NO atmosphere rather than the case in which the
thermal annealing process is conducted in the N₂O
25 atmosphere. Further, FIG.6 indicates that the N atoms
thus introduced are primarily concentrated in the
vicinity of the interface between the gate oxide film
13 and the substrate 11. In other words, the N atoms
introduced in the step of FIG.5C into the gate oxide
30 film 13 tend to show a concentration to the interface
to the substrate 11. It will be noted that the peak
concentration level of the N atoms in the gate oxide
film 13 is in the range of about 0.5% to about 2% or
more.

35 In the present embodiment, the thermal
annealing process of FIG.5C in the NO or N₂O
atmosphere is carried out after the ion implantation

1 process for forming the diffusion regions 11B and 11C.
This, however, is not a mandatory condition and it is
also possible to carry out the thermal annealing
process before the ion implantation process. In this
5 case, however, it is necessary to carry out a separate
thermal annealing process for activating the
introduced impurity elements in the diffusion regions
11B and 11C.

10 [SECOND EMBODIMENT]

FIGS.7A - 7G show the fabrication process of a MOS transistor according to a second embodiment of the present invention.

Referring to FIG.7A, a Si substrate 21 corresponding to the Si substrate 1 of FIG.1A is formed with a well 21a of the p-type or n-type, and a field oxide film 22 is formed on the substrate 21 by a wet oxidation process with a thickness of typically 300 - 400 nm, such that the field oxide film 22 defines a device region 21A on the surface of the substrate 21. Further, a thermal oxide film 23 is formed on the substrate 21 so as to cover the device region 21A with a thickness of typically 6 nm.

Further, in the step of FIG.7B, a
25 polysilicon film 24 corresponding to the polysilicon
film 4 of FIG.1B is deposited on the structure of
FIG.7A typically with a thickness of about 15 nm by a
CVD process conducted at a temperature of 800 - 900°C.
The polysilicon film 24 thus formed is then subjected
30 to an anisotropic etching process such as an RIE
process in the step of FIG.7C and a gate electrode 24A
is formed.

In the step of FIG.7C, a p-type dopant such as B or an n-type dopant such as As or P is further introduced into the substrate 21 by an ion implantation process while using the gate electrode 24A as a mask, and diffusion regions 21B and 21C are

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1 formed in the substrate 21.

5 In the step of FIG.7C, the substrate 21 thus processed is subjected to an ion implantation process in which N^+ ions are introduced into the gate oxide film 23 while using the gate electrode 24A as a mask. In the ion implantation process of N^+ atoms, the acceleration voltage is set such that the N^+ atoms do not reach the substrate 21. For example, the acceleration voltage is set to 100 keV or less, and 10 the ion implantation may be made with a dose of 1 - 3 $\times 10^{14} \text{ cm}^{-2}$ such that substantially the entire dangling bonds in the film 23 are terminated.

15 Next, in the step of FIG.7D, a CVD- SiO_2 film 25 is deposited on the structure of FIG.7C by a CVD process conducted in the same CVD apparatus at a temperature of typically about 800 °C, with a thickness of about 100 nm.

20 Next, in the step of FIG.7E, the CVD- SiO_2 film 25 is subjected to an anisotropic etching process such as an RIE process acting substantially perpendicularly to the principal surface of the substrate 21, and side wall oxides 25A and 25B are formed at both lateral sides of the gate electrode 24A, similarly to the side wall oxides 5A and 5B of 25 FIG.1D. Further, by conducting an ion implantation process of the foregoing p-type or n-type dopant into the substrate 21 in the state that the gate electrode 24A carry the side wall oxides 25A and 25B, an LDD structure including diffusion regions 21B' and 21C' 30 having a higher impurity concentration level inside the diffusion regions 21B and 21C, are obtained.

35 Next, in the step of FIG.7F, an interlayer insulation film 26 of SiO_2 is deposited on the structure of FIG.7E with an appropriate thickness, and ohmic electrodes 27A and 27B are provided on the ^{As shown in} ^{Fig.7G} interlayer insulation film 26 in ohmic contact with the diffusion regions 21C and 21B respectively via

1 contact holes formed in the interlayer insulation film
26.

5 In the present embodiment, too, the process
of FIG.7C for introducing the N atoms into the gate
oxide film 23 is carried out while using the gate
electrode 24A as a mask. Thus, the incorporation of
the N atoms does not occur in the part of the gate
oxide film 23 located immediately underneath the gate
electrode 24A and hence covering the channel region.
10 Thus, no substantial change or modification occurs in
the threshold characteristic or flat-band
characteristic of the MOS transistor even when the N
atoms are introduced into the gate oxide film 23.

15 As the N atoms are introduced with a high
concentration level selectively into the part of the
gate oxide film 23 corresponding to the drain edge
where the creation of the hot-carriers is most
prominent, the dangling bonds in the SiO_2 structure
forming the gate oxide film 23 are effectively
20 terminated, and the sites for trapping hot-carriers
are annihilated. Thus, the problem of trapping of the
electrons or holes by the gate oxide film 23 is
successfully avoided.

25 FIG.8 shows, by a thick continuous line
designated by "X," the degradation or variation ΔI_d of
a drain current I_d with a stress time, for a 64M bit
DRAM that uses the MOS transistor of FIG.5G. Further,
FIG.8 shows also a similar change of the drain
current, by open circles and designated as "REF," for
30 the case in which the MOS transistor is formed without
incorporation of N atoms into the gate oxide film.
Further, FIG.8 shows by solid circles the change of
the drain current I_d for the case in which the gate
oxide film is annealed in an oxygen atmosphere. In
35 any of the cases, the gate oxide film of the MOS
transistor has a thickness of about 10 nm.

Referring to FIG.8, it should be noted that

1 the variation or degradation of the drain current ΔI_d with time is significantly suppressed by incorporating the N atoms into the gate oxide film excluding the region located immediately underneath the gate electrode.

5 Further, the present invention is not limited to the embodiments described heretofore, but various variations and modifications may be made without departing from the scope of the invention.

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